AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the~~ steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plurality of~~plural~~ circuit cells, a switch for performing switching between ~~the~~ supply and non-supply of the first potential to each of semiconductor substrate areas of the plurality of~~plural~~ circuit cells, a second wiring for supplying a signal for controlling ~~the~~ operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells; and

(b) invalidating ~~the~~ function of the switch and connecting the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells is fixed to the power supply potential.

2. (Currently amended) The method according to claim 1, wherein each of the ~~respective~~ semiconductor substrate areas of the plurality of~~plural~~ circuit cells includes~~include~~ a semiconductor substrate area of first conductivity type, and a semiconductor substrate area of second conductivity type is opposite to the first conductivity type, the switch has a p channel type field effect transistor and an n channel type field effect transistor, the second wiring has one~~a second~~ wiring for the

p channel type field effect transistor and anothera ~~second~~ wiring for the n channel type field effect transistor, and the third wiring includes wirings for the first conductivity type semiconductor substrate area and the second conductivity type semiconductor substrate area.

3. (Original) The method according to claim 1, wherein the second wiring and the third wiring, and the first wiring are connected within an internal circuit area.

4. (Original) The method according to claim 1, wherein the second wiring and the third wiring, and the first wiring are connected within a peripheral circuit area.

5. (Currently amended) The method according to claim 1, wherein the plurality of~~plural~~ circuit cells are formed with memory cells and logic gates or input/output circuits.

6. (Currently amended) The method according to claim 1, further comprising a step of separating the second and third wirings from each other by a first circuit cell group that needs not supply the third potential, of the plurality of~~plural~~ circuit cells, and a second circuit cell group that needs supply the third potential, of the plurality of~~plural~~ circuit cells, wherein said (b) step is effected on the second and third wirings connected to the first circuit cell group.

7. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the~~ steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plurality of~~plural~~ circuit cells, a switch for performing switching between ~~the~~ supply and non-supply of the first potential to each of semiconductor substrate areas of the plurality of~~plural~~ circuit cells, a second wiring supplying a signal for controlling ~~the~~ operation of the switch and having a portion intersecting the first wiring, and a third wiring supplying the first potential or a third potential higher than the first potential, and having a portion intersecting the first wiring and being connected to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells; and

(b) invalidating ~~the~~ function of the switch, and connecting the second wiring to the first wiring at the point intersecting the first wiring and connecting the third wiring to the first wiring at a~~the~~ point intersecting the first wiring, such that the potential supplied to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells is fixed to the power supply potential.

8. (Original) The method according to claim 7, wherein the second wiring and the third wiring, and the first wiring are connected within an internal circuit area.

9. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the~~ steps of:

(a) preparing design data of the semiconductor device having an internal circuit area, a plurality of circuit cells disposed in the internal circuit area, a first wiring for supplying a first potential corresponding to a power supply potential to the plurality of~~plural~~ circuit cells, a first switch for performing switching between ~~the~~

supply and non-supply of the first potential to each of semiconductor substrate areas of the plurality of~~plural~~ circuit cells, a plurality of input/output circuit cells disposed around the internal circuit area, a second switch disposed in each of the plural input/output circuit cells and for performing switching between ~~the~~ supply and non-supply of the first potential to each of semiconductor substrate areas of the input/output circuit cells, a second wiring for supplying a signal for controlling ~~the~~ operation of each of the first and second switches, and a third wiring supplying the first potential or a third potential higher than the first potential and connected to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells and the plurality of~~plural~~ input/output circuit cells; and

(b) invalidating ~~the~~ functions of the first and second switches, and connecting the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells and the plurality of~~plural~~ input/output circuit cells is fixed to the power supply potential.

10. (Original) The method according to claim 9, wherein the second wiring and the third wiring, and the first wiring are connected within a peripheral circuit area.

11. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the~~ steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plurality of~~plural~~ circuit cells, a switch for performing switching between ~~the~~ supply and non-supply of the first potential to each of semiconductor

substrate areas of the plurality of~~plural~~ circuit cells, a second wiring for supplying a signal for controlling ~~the~~ operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells;

(b) separating the second and third wirings from each other by a first circuit cell group that needs not supply the third potential, of the plurality of~~plural~~ circuit cells, and a second circuit cell group that needs supply the third potential, of the plurality of~~plural~~ circuit cells; and

(c) invalidating ~~the~~ function of the switch with respect to the first circuit cell group, and connecting the second wiring and the third wiring connected to the first circuit cell group to the first wiring such that the potential supplied to each of semiconductor substrate areas of the first circuit cell group is fixed to the power supply potential.

12. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the~~ steps of:

(a) preparing design data of the semiconductor device having a plurality of field effect transistors, a first wiring for supplying a first potential corresponding to a power supply potential to the plurality of~~plural~~ field effect transistors, a switch for performing switching between ~~the~~ supply and non-supply of the first potential to each of semiconductor substrate areas of the plurality of~~plural~~ field effect transistors, a second wiring for supplying a signal for controlling ~~the~~ operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plurality of~~plural~~ field effect transistors;

(b) separating the second and third wirings from each other by a first field effect transistor group that needs not supply the third potential, of the plurality of~~plural~~ field effect transistors, and a second field effect transistor group that needs supply the third potential, of the plurality of~~plural~~ field effect transistors; and

(c) invalidating ~~the~~ function of the switch with respect to the first field effect transistor group, and connecting the second wiring and the third wiring connected to the first field effect transistor group to the first wiring such that the potential supplied to each of semiconductor substrate areas of the first field effect transistor group is fixed to the power supply potential.

13. (Original) The method according to claim 12, wherein the second field effect transistor group is lower in threshold value than the first field effect transistor group.

14. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the~~ steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plurality of~~plural~~ circuit cells, a switch for performing switching between ~~the~~ supply and non-supply of the first potential to each of semiconductor substrate areas of the plurality of~~plural~~ circuit cells, a second wiring for supplying a signal for controlling ~~the~~ operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells; and

(b) invalidating ~~the~~ function of the switch, and disposing, instead of the switch, a connecting cell having information for connecting the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plurality of~~plural~~ circuit cells is fixed to the power supply potential.

15. (Original) The method according to claim 14, wherein the connecting cell is disposed within an internal circuit area.

16. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the~~ steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit portions, a plurality of power supply switches respectively connected to the plurality of~~plural~~ circuit portions and for respectively performing switching between ~~the~~ supply and non-supply of a power supply potential to the plurality of circuit portions, and power supply switch control means for controlling ~~the~~ operations of the plurality of~~plural~~ power supply switches;

(b) separating a~~the~~ power supply switch connected to the always operation-desired circuit portion of the plurality of~~plural~~ circuit portions from the power supply switch control means; and

(c) fixing the input of the power supply switch connected to the always operation-desired circuit portion to the power supply potential.

17. – 27. (Cancelled).